# Summary

## Hall A – GEM

*Mary Ann Antonioli, Peter Bonneau, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen*

- Generated two Visio drawings – gas flow readout software flowchart and gas flow readout software diagram

## Hall A – SoLID

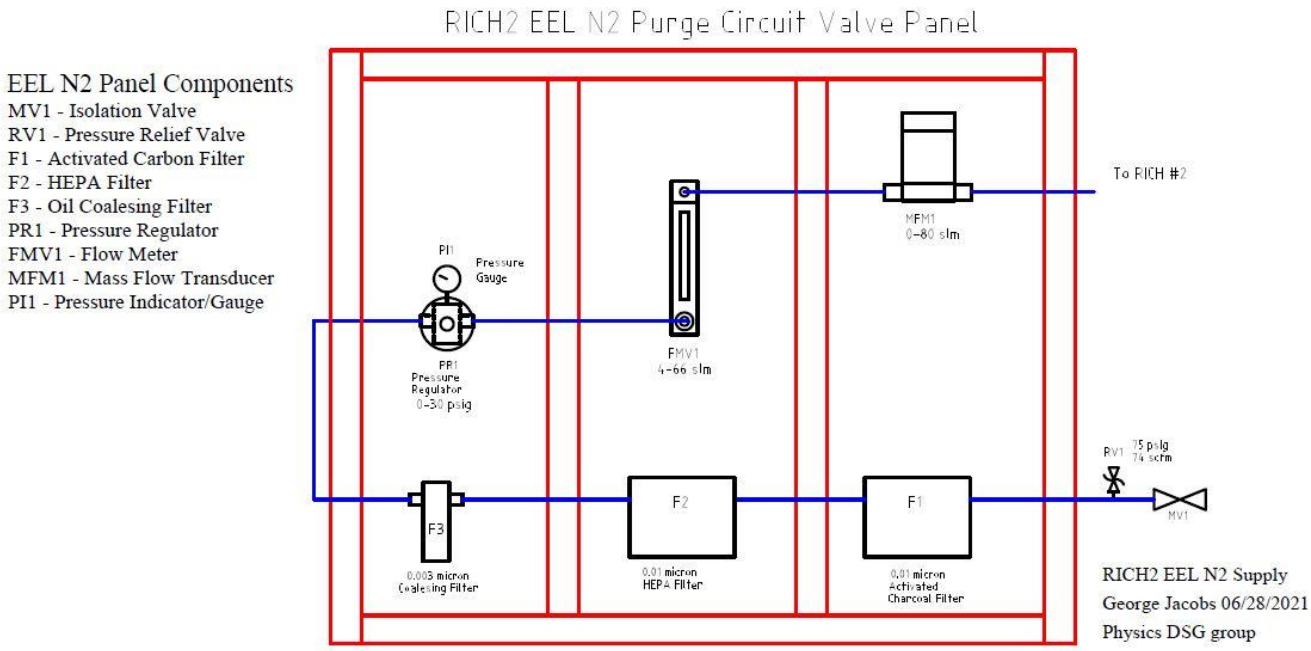
*Mary Ann Antonioli, Pablo Campero, Mindy Leffel, Marc McMullen*

- Populated both motor controller boards

## Hall B – RICH-II

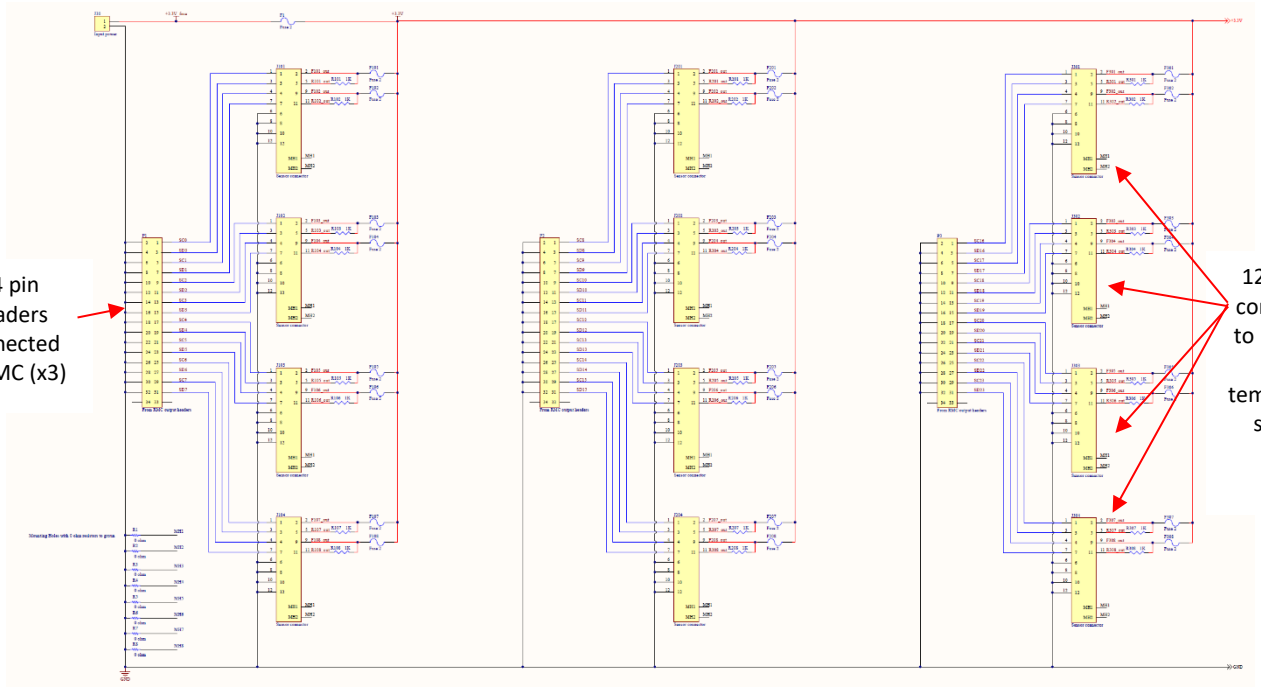
*Mary Ann Antonioli, Peter Bonneau, Pablo Campero, Tyler Lemon*

- Generated components diagram and spreadsheet for RICH-II $N_2$ purge system




Components diagram for RICH-II $N_2$ purge system

- Completed schematic for backplane PCB

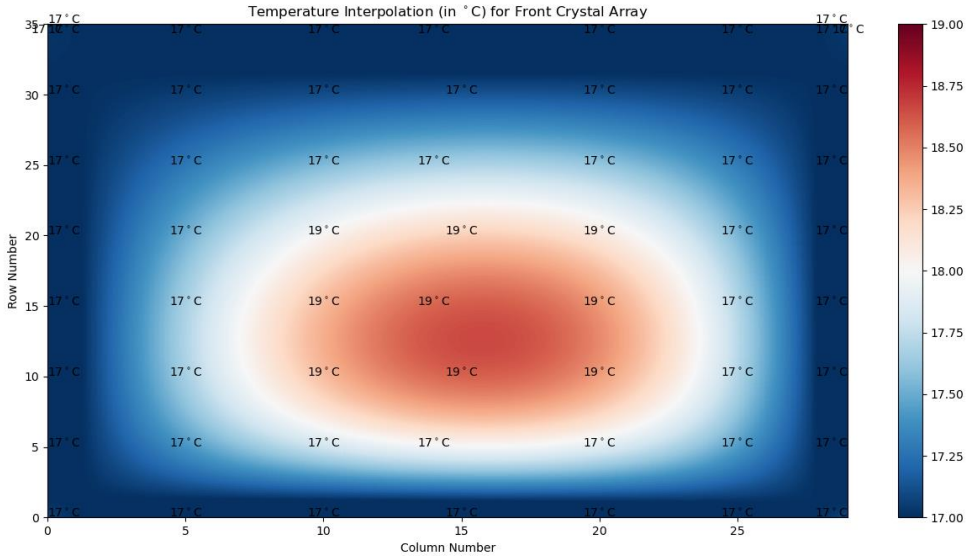



First of two pages for the backplane PCB schematic. Total number of 34-pin headers is 6 and total number of 12-pin headers is 24.

## Hall C – NPS

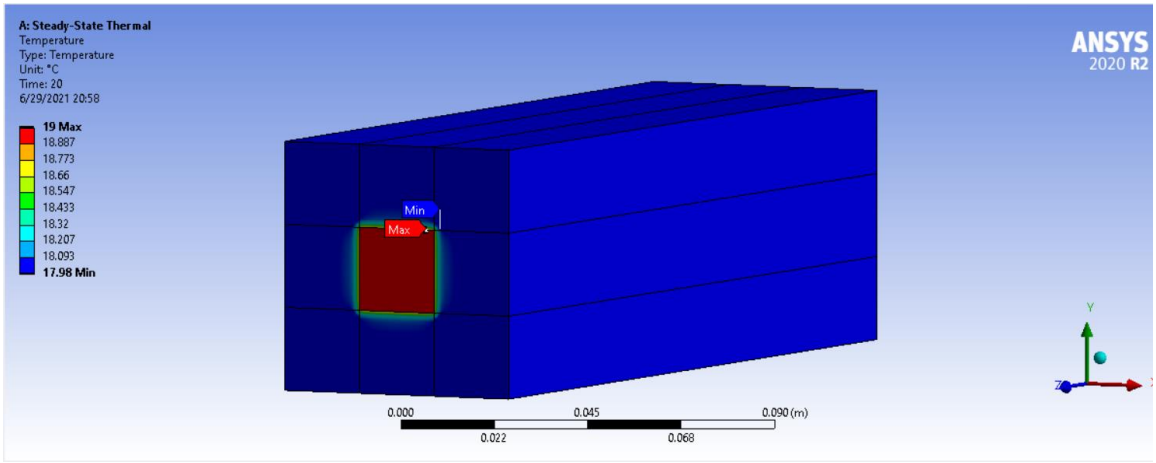
*Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, George Jacobs, Mindy Leffel, Tyler Lemon, Marc McMullen*

- Modified Python code to generate a bivariate spline interpolation for the front crystal zone temperatures
  - ✶ Changed the majority of temperature values to be 17°C and added a 3x3 block of values at 19°C

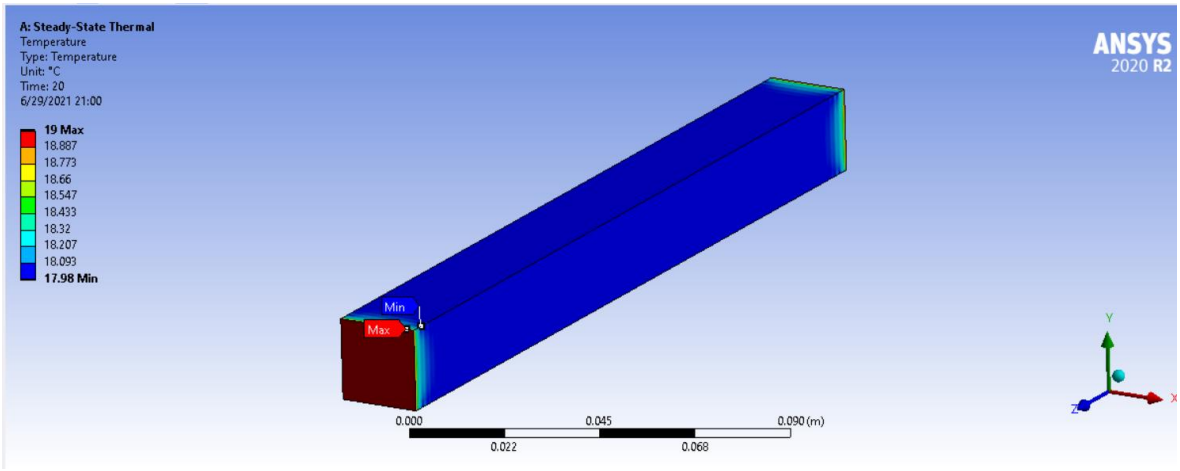



Plot of 3x3 block of temperature values at 19°C surrounded by temperature values of 17°C

- Using ANSYS, conducted a thermal analysis of a 3x3 block of $PbWO_4$ crystals
  - ✶ A heat of 19°C was applied to the front and back of the central crystal




Screenshot of ANSYS thermal simulation of 3x3 block of crystals; heat applied to central crystal




Screenshot of central crystal from ANSYS thermal simulation with 19°C applied to front and back

- Developed LabVIEW subVI to change cooling circuit temperature's indicator color based on input limits
- Received the majority of components ordered for the Hardware Interlock System
  - ✶ cRIO chassis and the ADC module are due on July 2nd
- Long-term load testing of HV supply cables: 33 cables complete
- Developing HV supply cable fabrication procedure
- Completed wiring the HV supply cable test load box and tested continuity

## EIC

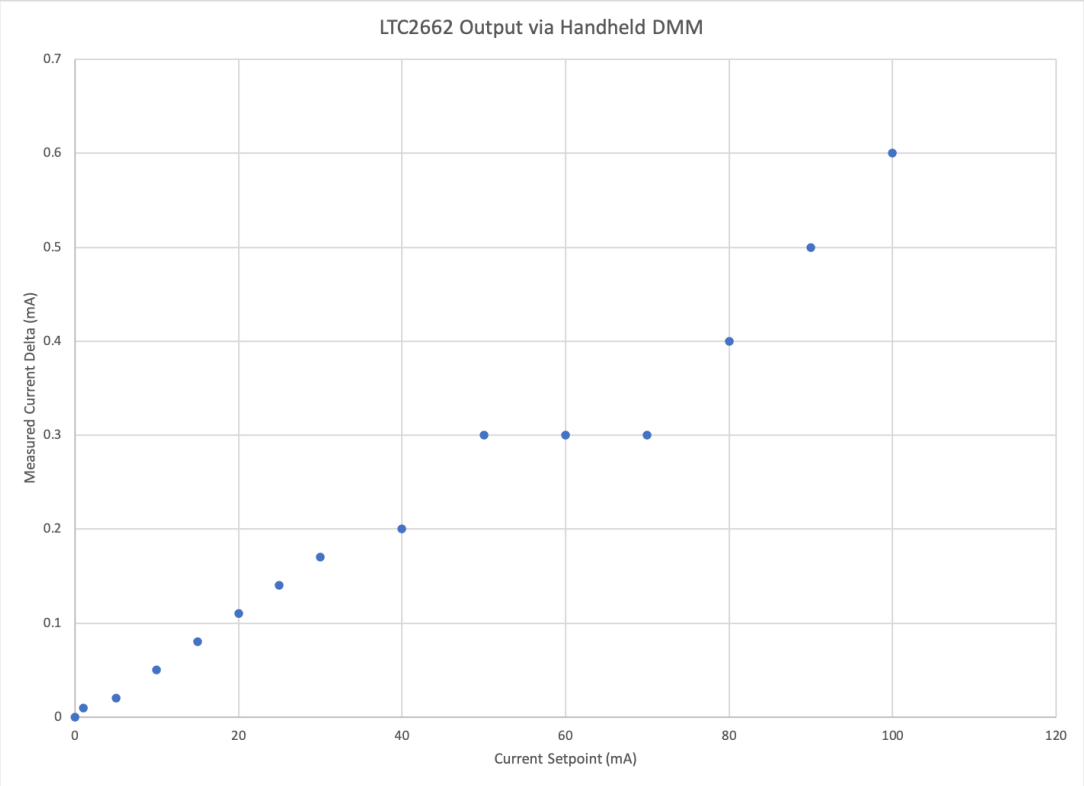
*Brian Eng*

- Attended the ATHENA tracking WG (working group) meeting
- Reviewed baseline detectors – alternative design with three tracking layers

## DSG R&D - GEM

*Brian Eng*

- Added code to communicate with a single LTC2662 (0-300 mA current output DAC) via SPI; measured output with a Fluke DMM




Plot of ΔI between set current using LTC2662 output DAC and measured current using Fluke DMM